

MAY 18 2007

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
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PATENT APPLICATION

ATTORNEY DOCKET NO. 10014268-1

Inventor(s): Robin Alexis Takasugi et al.

Confirmation No.:

Application No.: 10/672,975

Examiner: Sheng Jen Tsai

Filing Date: September 26, 2003

Group Art Unit: 2186

Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE
DEVICE

Mail Stop Amendment
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- ☐ Response/Amendment
☐ New fee as calculated below
☐ No additional fee
☒ Other Response to Non-Compliant Appeal Brief (8 pgs.). Fee\$ 0
- ☐ Petition to extend time to respond
☐ Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	30	MINUS	30	= 0	X \$50	\$ 0
INDEP. CLAIMS	4	MINUS	4	= 0	X \$200	\$ 0
<input type="checkbox"/> FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$360	\$ 0
EXTENSION FEE	<input type="checkbox"/> 1st Month \$120	<input type="checkbox"/> 2nd Month \$450	<input type="checkbox"/> 3rd Month \$1020	<input type="checkbox"/> 4th Month \$1590		\$ 0
OTHER FEES						\$ 0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this paper is being
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facsimile number (571) 273-8300.
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Typed Name: Jeff A. Holmen

Signature: Jeff A. Holmen

Respectfully submitted,

Robin Alexis Takasugi et al.

By Jeff A. Holmen

Jeff A. Holmen

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Rev 10/05 (TransAmrFax)

MAY 18 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

Applicant:	Robin Alexis Takasugi et al.	Examiner:	Sheng Jen Tsai
Serial No.:	10/672,975	Group Art Unit:	2186
Filed:	September 26, 2003	Docket No.:	10014268-1 / H303.154.101
Due Date:	May 19, 2007		
Title:	PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE		

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief mailed April 19, 2007, please consider the following remarks and the attached Revised Summary of Claimed Subject Matter:

Response to Non-Compliant Appeal Brief

Applicant: Robin Alexis Takasugi et al.

Serial No.: 10/672,975

Filed: September 26, 2003

Docket No.: 10014268-1 / H303.154.101

Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

REVISED SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1, 12, 17, and 20, and dependent claim 19. Discussions about elements of claims 1, 12, 17, 19, and 20 can be found at least at the cited locations in the specification and drawings.

The present invention, as claimed in independent claim 1, provides a prefetch controller for controlling retrieval of data from a data storage device in response to a current host command received from a host device. The prefetch controller includes a sequential read detector configured to generate a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential. A transfer length generator is configured to provide a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, thereby requesting data specified by the current host command and prefetch data, and provide a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command. The first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command. (See, e.g., specification at page 4, line 10 to page 14, line 24; Figures 1, 2, and 4; reference numbers 102, 104, 106, 116A-1, 118, and 206).

In addition to the above concise explanation, a more concise explanation of specific features can be found at, for example, the specification at page 11, lines 1-10. As set forth therein, during each command execution cycle, the prefetch length value output by multiplexer 408 and the transfer length value stored in register 414 are provided to adder 412, which adds the two received values, and outputs the sum to storage device interface 122 (Figure 1) via communication link 120A-1. The sum of the prefetch length value and the transfer length value represent the total transfer length value for the current host command. Thus, in one embodiment, for each READ command, a prefetch value is added by hardware to the transfer length value specified in the READ command, with the prefetch value varying depending upon whether the transfer is a new sequential READ or not. (Specification at page 11, lines 1-10).

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Applicant: Robin Alexis Takasugi et al.

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Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

The present invention, as claimed in independent claim 12, provides a method of transferring data between a host electronic device and a data storage device. The method includes receiving a current read command from the host electronic device. The current read command specifies a first transfer length value. The method includes identifying whether the current read command is non-sequential to a previously received read command. The method includes adding a prefetch length value to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value. The method includes outputting the second transfer length value to the data storage device. (See, e.g., specification at page 4, lines 10-16, and page 15, line 26 to page 17, line 5; Figures 1 and 6; reference numbers 102, 106, 602, 606, 610, and 614).

The present invention, as claimed in independent claim 17, provides a memory device including storage means (Figure 1, reference number 106; specification at page 4, lines 12-13) for storing data. The memory device includes host interface means (Figure 1, reference number 114; specification at page 5, lines 22-24) for receiving host commands from a host electronic device, sequential read detection means (Figure 2, reference number 206; specification at page 7, line 29 to page 8, line 2) for identifying whether a current host command specifies a non-sequential read operation, and transfer length generation means (Figures 1 and 4, reference number 118; specification at page 10, lines 13-26) for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation. The transfer length generation means is configured to output a sum of the prefetch length value and the transfer length value to the storage means. (See, e.g., specification at page 4, line 10 to page 14, line 24; Figures 1, 2, and 4; reference numbers 102, 104, 106, 114, 118, and 206).

In addition to the above concise explanation, a more concise explanation of specific features can be found at, for example, the specification at page 11, lines 1-10. As set forth therein, during each command execution cycle, the prefetch length value output by multiplexer 408 and the transfer length value stored in register 414 are provided to adder 412, which adds the two received values, and outputs the sum to storage device interface 122 (Figure 1) via communication link 120A-1. The sum of the prefetch length value and the transfer length value represent the total transfer length value for the current host command.

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Thus, in one embodiment, for each READ command, a prefetch value is added by hardware to the transfer length value specified in the READ command, with the prefetch value varying depending upon whether the transfer is a new sequential READ or not. (Specification at page 11, lines 1-10).

The present invention, as claimed in dependent claim 19, provides the memory device of claim 17, wherein the transfer length generation means comprises: **first register means** (Figure 4, reference number 404; specification at page 10, lines 11-12) for storing the prefetch length value; **second register means** (Figure 4, reference number 406; specification at page 10, line 13) for storing a zero value; **multiplexing means** (Figure 4, reference number 408; specification at page 10, lines 13-26) for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection means; and **adding means** (Figure 4, reference number 412; specification at page 11, lines 1-5) for adding an output of the multiplexing means and the transfer length value specified in the current host command. (See, e.g., specification at page 4, line 10 to page 14, line 24; Figures 1, 2, and 4; reference numbers 102, 104, 106, 114, 118, 206, 404, 406, 408, and 412).

In addition to the above concise explanation, a more concise explanation of specific features can be found at, for example, the specification at page 10, lines 13-26. As set forth therein, during each command execution cycle, the values stored in registers 404 and 406 are both provided to multiplexer 408, which outputs one of the two values to adder 412 based on a signal received on communication link 116A-1 from sequential read logic 308 (Figure 3). In one embodiment, if sequential read logic 308 outputs a logically true new sequential read flag for the current host command to multiplexer 408 via communication link 116A-1, multiplexer 408 outputs the value stored in prefetch register 404 to adder 412. If sequential read logic 308 outputs a logically false new sequential read flag for the current host command to multiplexer 408 via communication link 116A-1, multiplexer 408 outputs the value stored in zero register 406 to adder 412. Thus, the signal output by sequential read logic 308 selectively switches the multiplexer 408 to output either a non-zero prefetch value in the case of a potentially new sequential transfer, or a zero if the current transfer is not a new sequential transfer. (Specification at page 10, lines 13-26).

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The present invention, as claimed in independent claim 20, provides a computer-readable medium having computer-executable instructions for performing a method of transferring data between a host electronic device and a data storage device. The method includes receiving a current host command from the host electronic device, generating a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential, and outputting a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command. The first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command. The method includes outputting a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command. The second transfer length value is less than the first transfer length value. (See, e.g., specification at page 4, lines 10-16, and page 15, line 26 to page 17, line 5; Figures 1, 2, and 6; reference numbers 102, 106, 116A-1, 602, 606, 608, 610, and 614).

REMARKS

The Examiner stated in the Notification of Non-Compliant Appeal Brief mailed on April 19, 2007 that:

The appeal brief fails to provide a concise [sic] explanation of the subject matter defined in each of the independent claims involved in the appeal.

For independent claim 1, the appeal brief refers claimed limitations to page 4, line 10 through page 14, lines 24 of the Specification. Giving the fact that the Specification has only 17 pages, the passage cited for the explanation of the particular subject matter is almost the entire Specification itself, and fails to provide a concise explanation.

Independent claim 17 and dependent claim 19 also refer [sic] claimed limitations to page 4, line 10 through page 14, lines 24 of the Specification, thus suffer from the same defect. (Notification at page 2).

Appellant is not aware of any statute or rule that requires the Summary to cite less than 10 pages of the specification. Appellant is also not aware of any statute or rule that requires that the Summary cite less than 59% (10 pages divided by 17 pages) of the specification. Nonetheless, to facilitate an efficient prosecution of the present Appeal,

Response to Non-Compliant Appeal Brief

Applicant: Robin Alexis Takasugi et al.

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Appellant has submitted herewith a Revised Summary of Claimed Subject Matter pursuant to MPEP § 1205.03, which adds a "more concise explanation" for claims 1, 17, and 19.

CONCLUSION

Any inquiry regarding this Response should be directed to either Nathan Rieth at Telephone No. (208) 396-5287, Facsimile No. (208) 396-3958 or Jeff A. Holmen at Telephone No. (612) 573-0178, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Hewlett-Packard Company
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P.O. Box 272400
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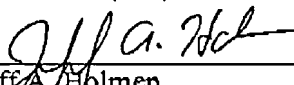
Respectfully submitted,

Robin Alexis Takasugi et al,

By their attorneys,

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Dated: 5/18/07
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Jeff A. Holmen
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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via telefacsimile to Fax No. (571) 273-8300 on this 18th day of May, 2007.

By: Name: Jeff A. Holmen